REMARKS/ARGUMENTS

In this amendment, the specification and claims 6 and 14 are amended, and claims 1-5, 12, 13, and 16-19 are cancelled. The specification is amended according to the Examiner's suggestion on page 4 to replace the "□" symbols on page 2 with the appropriate =, +, and * symbols. Claims 6 is amended to incorporate the subject matter of claims 12 and 13. Claim 14 is amended to incorporate the subject matter of claims 16-19. In other words, claim 6 is amended to correspond in scope to pending claim 13, and claim 14 is amended to correspond in scope to pending claim 14. No new matter is introduced. No new issues are presented for the examiner's consideration which would prevent entry of these amendments under 37 CFR 1.116. Applicants respectfully request entry and favorable consideration of the foregoing amendments.

Applicants express appreciation to Examiner Chaudry for discussing this application with Applicants' attorney on June 23, 2006 and August 24, 2006. During those discussions, the pending claims and the cited prior art were discussed, including the Itakura et al. and Katsuragawa et al. patents and an excerpt from Stephen B. Wichker, *Error control Systems*, "12.4.3 The Branch Metric Computer." It was noted that none of the prior art of disclosed the branch metric calculating operations described in paragraph [0031] of the specification. Paragraph [0031] defines the branch metric calculating operations of the consecutive data according to a plurality of target level sets as follows: "the differences of the input data with all the corresponding target values are squared to obtain a plurality of branch metric values." Paragraph [0031] further provides an example of the branch metric calculating operations assuming two consecutive data y(k) and y(k-1) and two target level sets (2, 1, 0, -1, -2) and (1.5, 1, 0, -1, -1.5). "Then, branch metric values (y(k)-2)^2, (y(k)-1)^2, (y(k))^2, (y(k)+1)^2, (y(k)+2)^2, (y(k-1)-1.5)^2, (y(k-1)-1)^2, (y(k-1))^2, (y(k-1)+1)^2, (y(k-1)+1.5)^2 are obtained, as shown in Fig. 7." See also Paragraph [0033]. None of the prior art of record discloses the foregoing branch metric calculating operations, particularly the identified target level sets (2, 1, 0, -1, -2) and (1.5, 1, 0, -1, -1.5) recited in claims 13 and 19.

Claim Rejections – 35 USC § 103. The Office Action rejected claims 1-19 under Section 103(a) as being unpatentable over Katsuragawa et al. (USPN 5907586; hereinafter Katsuragawa) in view of Itakura et al. (USPN 5418795; hereinafter Itakura). In view of the currently pending

claims, the Applicants respectfully traverse the rejection for the following reasons.

The Applicants submit that Katsuragawa in view of Itakura fails to teach or suggest that a plurality of consecutive input data are branch metric calculated according to a plurality of target level sets, respectively, ***wherein said target level sets are obtained via a partial response channel PR(1,1,1,1) and are (-2,-1,0,1,2) and (-1.5,-1,0,1,1.5)***. It was agreed during the telephonic interview that the cited prior art does not disclose these features.

The Office Action, pages 2-3, refers to Itakura's add-compare-select-state-metric ("ACS-SM") normalization circuit **4** as teaching the use of multiple target levels in performing branch metric calculating operations. However, Itakura's ACS-SM is not a branch metric calculating circuit. Even the pending claims distinguish the "adder-comparator-selector unit" from the "branch metric calculating circuit." Itakura's ACS-SM has nothing to do with "performing branch metric calculation operations on two consecutive input data according to two sets of target levels, respectively, to obtain a plurality of branch metric values" as recited in the claims. Itakura discloses a branch metric calculation circuit **101**, but does not disclose the arithmetic operations performed by the branch metric calculation circuit **101**, and clearly does not disclose the use of the two target level sets, (-2,-1,0,1,2) and (-1.5,-1,0,1,1.5), recited in the amended claims.

The Katsuragawa patent discloses a system utilizing a "plurality of Viterbi decoders" in contrast to the present invention which utilizes a single Viterbi decoding device and method capable of processing multi-data input into multi-data ouput. See, Paragraph [0007]. Katsuragawa refers to a branch metric compute circuit **450**. Like Itakura, Katsuragawa does not disclose the arithmetic operations performed by the branch metric calculation circuit **450**, and fails to disclose the use of the two target level sets recited in the amended claims.

Because the prior art references in combination fail to teach or suggest all the claim limitations, the Applicants submit that the pending claims would not have been obvious from the cited references. Applicants request withdrawal of the rejection and allowance of the claims. If there are any remaining issues preventing allowance of the pending claims that may be clarified by telephone, the Examiner is requested to call the undersigned.

Respectfully submitted,

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